HANDLING PROCESSOR INTERNAL ERRORS IN AN SMP SERVER

ABSTRACT

A system and method for handling processor internal errors in a data processing system. The data processing system typically includes a set of main microprocessors that have access to a common system memory via a system bus. The system may further include a service processor that is connected to at least one of the main processors. In addition, the system includes internal error handling hardware configured to log and process internal errors generated by one or more of the main processors. The internal error hardware may include error detection logic configured to receive internal error signals from the main processors. In response to receiving one or more IERR signals, the error detection logic is configured to assert and error detected signal that is received by error logging logic. The error logging logic is configured to update one or more error status register when the error detected signal is asserted. When the error logging logic has updated the status registers, is configured to assert an error logging complete signal that is received by processing control logic. The processor control logic is configured to assert one or more processor enable signals based on the state of the error status registers. In addition, upon completion of the error status update by the error logging logic, the status register is configured to assert an error status updated signal that ultimately produces a system reset. By incorporating error logging and handling into dedicated hardware tied directly to the processor internal error signals, the invention provides a low cost, low response latency mechanism for handling processor internal errors in high performance multiprocessor systems.